USBMOD245R - USB to Parallel FIFO Development Module

The USBMOD245R shown in Diagram 1, is the latest RoHS compliant, low-cost integrated module for transferring data to / from a peripheral to a host PC via USB. The module is based on the FT245R USB to Parallel FIFO IC from FTDI. It's simple FIFO-like design makes it easy to interface to a CPU (MCU) either by mapping the device into the memory / I/O map of the CPU, using DMA or controlling the device via I/O ports.

The USBMOD245R offers a complete plug and play solution for implementing the FT245R into both new and existing designs, which makes the module ideal for rapid prototyping and development.

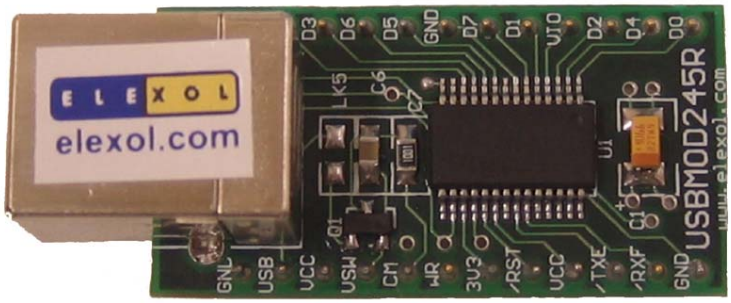


Diagram 1

MODULE FEATURES

- Single module High-Speed USB Parallel FIFO solution that is based on the FTDI FT245R USB IC
- Integrated Type-B USB Connector
- RoHS Compliant
- No external passive components required
- Module can be configured for both External and Bus powered operation.
- On board power switching circuit for high bus powered applications
- 24-pin Dual In-Line Package (Ideal for prototyping)

FT245R FEATURES

- Single chip USB to parallel FIFO bidirectional data transfer interface.
- Entire USB protocol handled on the chip - No USB-specific firmware programming required.
- Simple interface to MCU / PLD / FPGA logic with simple 4-wire handshake interface.
- Data transfer rate to 1 Megabyte / second - D2XX Direct Drivers.
- Data transfer rate to 300 kilobyte / second - VCP Drivers.
- FTDI's royalty-free VCP and D2XX drivers eliminate the requirement for USB driver development in most cases.
- New USB FTDIChip-ID™ feature.
- FIFO receive and transmit buffers for high data throughput.
- Adjustable receive buffer timeout.
- Synchronous and asynchronous bit bang mode interface options with RD# and WR# strobes allow the data bus to be used as a general purpose I/O port.
- Integrated 1024 Bit internal EEPROM for storing USB VID, PID, serial number and product description strings.
- Device supplied pre-programmed with unique USB serial number.
- Support for USB suspend / resume through PWREN# pin and Wake Up pin function.
- In-built support for event characters.
- Support for bus powered, self powered, and high-power bus powered USB configurations.
- Integrated 3.3V level converter for USB I/O .
- Integrated level converter on FIFO interface and control pins for interfacing to 5V - 1.8V Logic.
- True 5V / 3.3V / 2.8V / 1.8V CMOS drive output and TTL input.
- High I/O pin output drive option.
- Integrated USB resistors.
- Integrated power-on-reset circuit.
- Fully integrated clock - no external crystal, oscillator, or resonator required.
- Fully integrated AVCC supply filtering - No separate AVCC pin and no external R-C filter required.
- USB bulk transfer mode.
- 3.3V to 5.25V Single Supply Operation.
- Low operating and USB suspend current.
- Low USB bandwidth consumption.
- UHCI / OHCI / EHCI host controller compatible
- USB 2.0 Full Speed compatible.
- -40°C to 85°C extended operating temperature range.
- Available in compact Pb-free 28 Pin SSOP and QFN-32 packages (both RoHS compliant).

FT245R ENHANCEMENTS

This section summarises the enhancements and the key features of the FT245R device. For further details, on the FT245R consult the FT245R datasheet that is available for download from the FTDI website. (http://www.ftdichip.com)

Integrated Clock Circuit - Previous generations of FTDI's USB to parallel FIFO interface devices required an external crystal or ceramic resonator. The clock circuit has now been integrated onto the device meaning that no crystal or ceramic resonator is required. However, if required, an external 12MHz crystal can be used as the clock source.

Integrated EEPROM - Previous generations of FTDI's USB to parallel FIFO interface devices required an external EEPROM if the device were to use USB Vendor ID (VID), Product ID (PID), serial number and product description strings other than the default values in the device itself. This external EEPROM has now been integrated onto the FT245R chip meaning that all designs have the option to change the product description strings. A user area of the internal EEPROM is available for storing additional data. The internal EEPROM is programmable in circuit, over USB without any additional voltage requirement.

Pre-programmed EEPROM - The FT245R is supplied with its internal EEPROM pre-programmed with a serial number that is unique to each individual device. This, in most cases, will remove the need to program the device EEPROM.

Integrated USB Resistors - Previous generations of FTDI's USB to parallel FIFO interface devices required two external series resistors on the USBDP and USBDM lines, and a 1.5 kΩ pull up resistor on USBDP. These three resistors have now been integrated onto the device.

Integrated AVCC Filtering - Previous generations of FTDI's USB to parallel FIFO interface devices had a separate AVCC pin - the supply to the internal PLL. This pin required an external R-C filter. The separate AVCC pin is now connected internally to VCC, and a filter is integrated onto the chip.

Less External Components - Integration of the crystal, EEPROM, USB resistors, and AVCC filter will substantially reduce the bill of materials cost for USB interface designs using the FT245R compared to its FT245BM predecessor.

Enhanced Asynchronous Bit Bang Mode with RD# and WR# Strobes - The FT245R supports FTDI's BM chip bit bang mode. In bit bang mode, the eight parallel FIFO data bus lines can be switched from the regular interface mode to an 8-bit general purpose I/O port. Data packets can be sent to the device and they will be sequentially sent to the interface at a rate controlled by an internal timer (equivalent to the baud rate prescaler). With the FT245R device, this mode has been enhanced so that the internal RD# and WR# strobes are now brought out of the device which can be used to allow external logic to be clocked by accesses to the bit bang I/O bus. This option will be described more fully in a separate application note

Synchronous Bit Bang Mode - Synchronous bit bang mode differs from asynchronous bit bang mode in that the interface pins are only read when the device is written to. Thus making it easier for the controlling program to measure the response to an output stimulus as the data returned is synchronous to the output data. The feature was previously seen in FTDI's FT2232C device. This option will be described more fully in a separate application note.

Lower Supply Voltage - Previous generations of the chip required 5V supply on the VCC pin. The FT245R will work with a VCC supply in the range 3.3V - 5V. Bus powered designs would still take their supply from the 5V on the USB bus, but for self powered designs where only 3.3V is available, and there is no 5V supply, there is no longer any need for an additional external regulator.

Integrated Level Converter on FIFO Interface and Control Signals - VCCIO pin supply can be from 1.8V to 5V. Connecting the VCCIO pin to 1.8V, 2.8V, or 3.3V allows the device to directly interface to 1.8V, 2.8V or 3.3V and other logic families without the need for external level converter I.C.s

5V / 3.3V / 2.8V / 1.8V Logic Interface - The FT245R provides *true* CMOS Drive Outputs and TTL level Inputs.

Integrated Power-On-Reset (POR) Circuit- The device incorporates an internal POR function. A RESET# pin is available in order to allow external logic to reset the FT245R where required. However, for many applications the RESET# pin can be left unconnected, or pulled up to VCCIO. FT245R USB UART I.C. Datasheet Version 1.02 © Future Technology Devices International Ltd. 2005 Page 4

Wake Up Function - If USB is in suspend mode, and remote wake up has been enabled in the internal EEPROM (it is enabled by default), the RXF# pin becomes an input. Strobing this pin low will cause the FT245R to request a resume from suspend on the USB bus. Normally this can be used to wake up the host PC from suspend

Lower Operating and Suspend Current - The device operating supply current has been further reduced to 15mA, and the suspend current has been reduced to around 70µA. This allows a greater margin for peripherals to meet the USB suspend current limit of 500µA.

Low USB Bandwidth Consumption - The operation of the USB interface to the FT245R has been designed to use as little as possible of the total USB bandwidth available from the USB host controller.

High Output Drive Option - The parallel FIFO interface and the four FIFO handshake pins can be made to drive out at three times the standard signal drive level thus allowing multiple devices to be driven, or devices that require a greater signal drive strength to be interfaced to the FT245R. This option is configured in the internal EEPROM.

Power Management Control for USB Bus Powered, High Current Designs- The PWREN# signal can be used to directly drive a transistor or P-Channel MOSFET in applications where power switching of external circuitry is required. An option in the internal EEPROM makes the device gently pull down on its FIFO interface lines when the power is shut off (PWREN# is high). In this mode any residual voltage on external circuitry is bled to GND when power is removed, thus ensuring that external circuitry controlled by PWREN# resets reliably when power is restored.

FTDIChip-ID™ - Each FT245R is assigned a unique number which is burnt into the device at manufacture. This ID number cannot be reprogrammed by product manufacturers or end-users. This allows the possibility of using FT245R based dongles for software licensing. Further to this, a renewable license scheme can be implemented based on the FTDIChip-ID™ number when encrypted with other information. This encrypted number can be stored in the user area of the FT245R internal EEPROM, and can be decrypted, then compared with the protected FTDIChip-ID™ to verify that a license is valid. Web based applications can be used to maintain product licensing this way. An application note describing this feature is available separately from the FTDI website.

Improved EMI Performance - The reduced operating current and improved on-chip VCC decoupling significantly improves the ease of PCB design requirements in order to meet FCC, CE and other EMI related specifications.

Programmable FIFO TX Buffer Timeout - The FIFO TX buffer timeout is used to flush remaining data from the receive buffer. This timeout defaults to 16ms, but is programmable over USB in 1ms increments from 1ms to 255ms, thus allowing the device to be optimised for protocols that require fast response times from short data packets.

Extended Operating Temperature Range - The FT232R operates over an extended temperature range of -40º to +85º C thus allowing the device to be used in automotive and industrial applications.

New Package Options - The FT245R is available in two packages - a compact 28 pin SSOP (**FT245RL**) and an ultra-compact 5mm x 5mm pinless QFN-32 package (**FT245RQ**). Both packages are lead (Pb) free, and use a 'green' compound. Both packages are fully compliant with European Union directive 2002/95/EC.

MODULE PINOUT & PIN DESCRIPTIONS

As mentioned above in module features, the USBMOD245R is in a 24-pin Dual In-Line Package that allows the module to fit into a standard 24-pin 600mil IC Socket, thereby making the module ideal for prototyping and development work.

Shown in Diagram 2 below is the pin out for the USBMOD245R.

USBMOD245R PINOUT

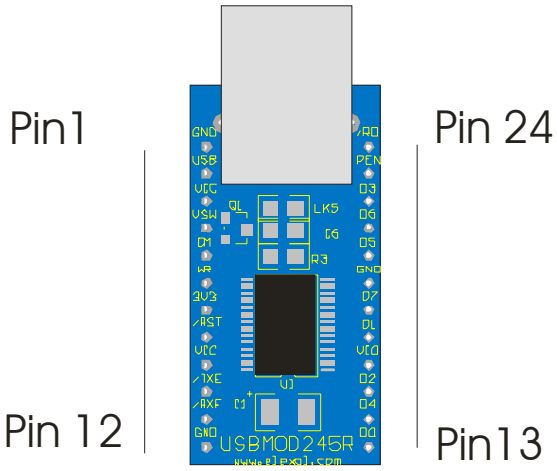


DIAGRAM 2

On the following page is the pin out table detailing the various pin functions on the module.

USBMOD245R PINOUT TABLE

PIN #	SIGNAL	TYPE	DESCRIPTION
1	GND	PWR	Device – Ground Supply Pin
2	USB	PWR	USB Bus Power
3	VCC	PWR	Device - +4.4 volt to +5.25 volt Power Supply Pin NOTE: No external voltage is required when Bus Powered
4	VSW	PWR	Switched Power supply pin for external devices. Is controlled via the CM pin which is connected to PEN, in bus powered mode with power switching. NOTE: No external voltage is required when Bus Powered
5	CM	IN	Connect to PEN to control the external power switching of external devices in USB bus powered operation
6	WR	IN	Writes the Data Byte on the D0..D7 pins in the Transmit FIFO Buffer when WR goes from high to low. For Further information see the timing diagrams
7	3V3	OUT	3.3 volt Output from the integrated L.D.O. regulator. Up to 50mA of current can be drawn from this pin to power external 3.3v logic if required.
8	/RST	IN	Can be used by external device to reset FT245R.
9	VCC	PWR	Device - +4.4 volt to +5.25 volt Power Supply Pin NOTE: No external voltage is required when Bus Powered
10	/TXE	OUT	When high, do not write data into the FIFO. When low, data can be written into the FIFO by strobing WR high then low. For Further information see the timing diagrams
11	/RXF	OUT	When high, do not read data from FIFO. When low, there is data available in the FIFO, which can be read by strobing /RD low the high again. For Further information see the timing diagrams
12	GND	PWR	Device – Ground Supply Pin
13	D0	I/O	Bi-Directional Data Bus Bit #0
14	D4	I/O	Bi-Directional Data Bus Bit #4
15	D2	I/O	Bi-Directional Data Bus Bit #2
16	VIO	PWR	+1.8V volt to +5.25 volt VCC to the FIFO interface pins. Placing LK4 (remove LK3) will power the FIFO pins to 3V3, otherwise place LK3 to drive out at 5v CMOS level. If driving other voltages via VIO be sure to remove both LK3 & LK4
17	D1	I/O	Bi-Directional Data Bus Bit #1
18	D7	I/O	Bi-Directional Data Bus Bit #7
19	GND	PWR	Device – Ground Supply Pin
20	D5	I/O	Bi-Directional Data Bus Bit #5
21	D6	I/O	Bi-Directional Data Bus Bit #6
22	D3	I/O	Bi-Directional Data Bus Bit #3
23	PEN	OUT	Goes Low after the device is configured via USB, then high during USB suspend. Can be connected to CM, to control power to external logic powered from VSW. Enable the Interface Pull-Down Option in EEPROM when using the /PEN pin in this way.
24	/RD	IN	Enables Current FIFO Data Byte on D0..D7 when low. Fetches the next FIFO Data Byte (if available) from the Receive FIFO Buffer when /RD goes from low to high. For Further information see the timing diagrams

FT245R FIFO TIMING DIAGRAMS

FIFO READ CYCLE

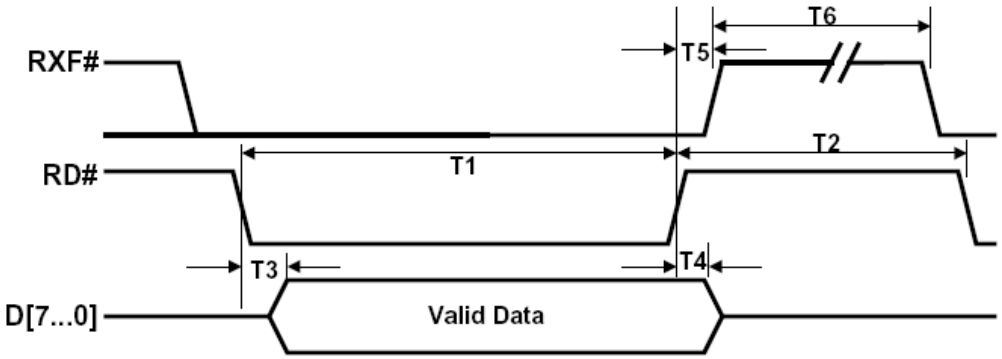


Image for FT245R FIFO Read cycle taken from the FT245R datasheet.
(http://www.ftdichip.com)

Time	Description	Min	Max	Unit
T1	RD Active Pulse Width	50		ns
T2	RD to RD Pre-Charge Time	50 + T6		ns
T3	RD Active to Valid Data	20	50	ns
T4	Valid Data Hold Time from RD Inactive with load of 30pF	0		ns
T5	RD Inactive to RXF#	0	25	ns
T6	RXF Inactive after RD Cycle	80		ns

FIFO WRITE CYCLE

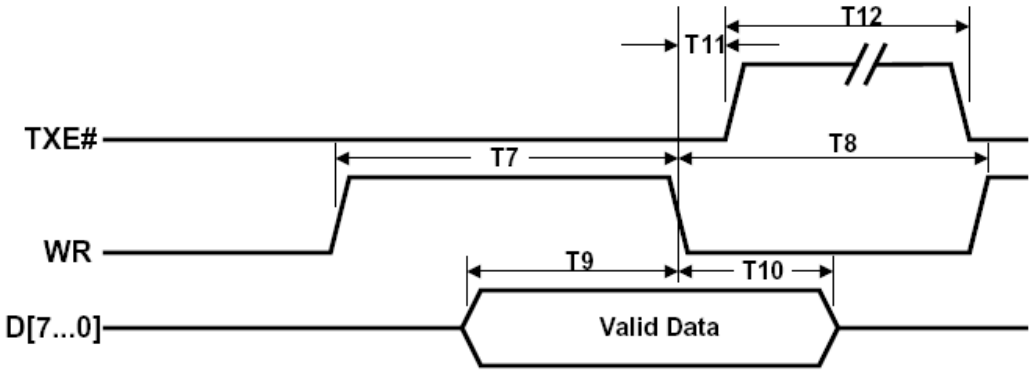


Image for FT245R FIFO Write cycle taken from the FT245R datasheet.
(http://www.ftdichip.com)

Time	Description	Min	Max	Unit
T7	WR Active Pulse Width	50		ns
T8	WR to WR Pre-Charge Time	50		ns
T9	Data setup time before WR Inactive	20		ns
T10	Data Hold Time from WR Inactive	0		ns
T11	WR Inactive to TXE#	5	25	ns
T12	TXE Inactive after WR Cycle	80		ns

MODULE CONFIGURATIONS

BUS POWERED OPERATION

The USBMOD245R is configured to be bus powered off the assembly line. There are no external pins that are required to be connected in order for the device to enumerate.

BUS POWERED OPERATION with Power switching

The USBMOD245R can be easily configured for bus powered operation with power switching.

1. Place LK5with 0R0
2. Set the Pull-down on suspend option in the internal EEPROM
3. Connect the PEN pin to CM pin
4. Make sure that the external logic that is being switched has its own reset circuitry so that it will automatically reset when coming out of suspend mode.

SELF POWERED OPERATION

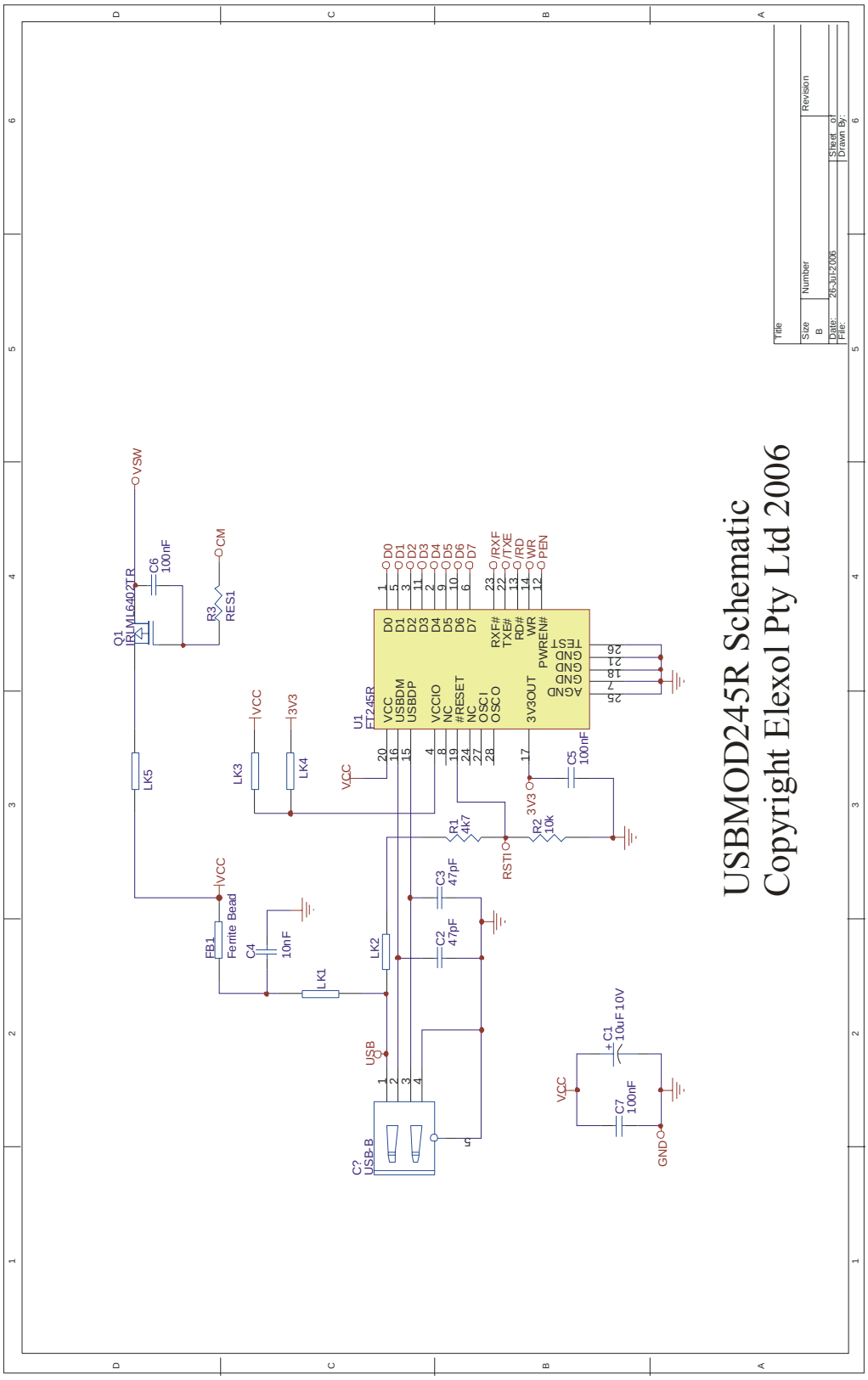
To self power the USBMOD245R the process is as follows:

1. Remove LK1 keep the 0R0 and move it LK2.
2. Place LK2 with the 0R0 taken from LK1.
3. Place R1 (4k7 0805) and R2 (10K 0805)
4. Connect VCC to an external 5V supply.

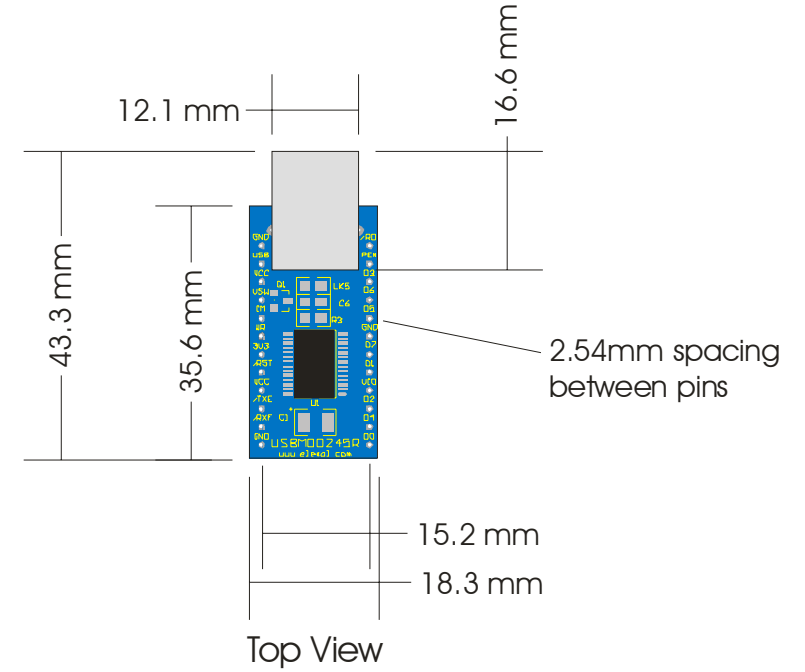
SCHEMATIC

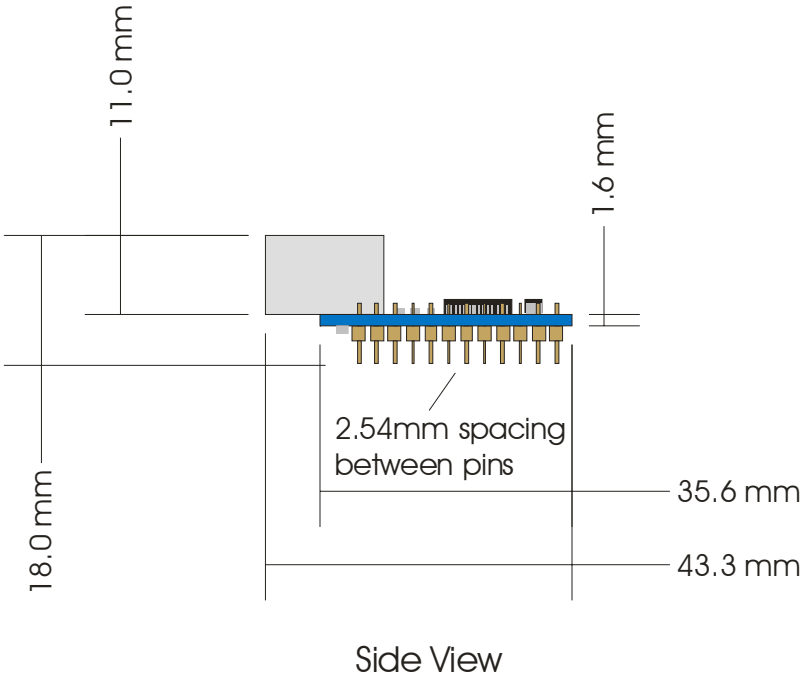
The following page shows the schematic for the USBMOD245R.

USBMOD245R SCHEMATIC



MECHANICALS





All dimensions are shown in millimeters.

The USBMOD245R uses all lead free components.

SOFTWARE DRIVERS

There are drivers available for the different operating systems which are listed below. These drivers are available to download for free from the FTDI website. **http://www.ftdichip.com**

Royalty-Free VIRTUAL COM PORT (VCP) DRIVERS for...

- Windows 98, 98SE, ME, 2000, Server 2003, XP.
- Windows Vista / Longhorn*
- Windows XP 64-bit.*
- Windows XP Embedded.
- Windows CE.NET 4.2 & 5.0
- MAC OS 8 / 9, OS-X
- Linux 2.4 and greater

Royalty-Free D2XX *Direct* Drivers (USB Drivers + DLL S/W Interface)

- Windows 98, 98SE, ME, 2000, Server 2003, XP.
- Windows Vista / Longhorn*
- Windows XP 64-bit.*
- Windows XP Embedded.
- Windows CE.NET 4.2 & 5.0
- Linux 2.4 and greater

* Currently Under Development. Contact FTDI for availability.

D2XX Programmers guide is also available for download from the FTDI website.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ……..	-65°C to + 150°C
Ambient Temperature (Power Applied)……...	-40°C to + 85°C
VCC Supply Voltage ……	-0.5V to +6.00V
DC Input Voltage – USBDP and USBDM…….	-0.5V to 3.8V
DC Input Voltage - High Impedance Bidirectionals …….	-0.5V to VCC + 0.5V
DC Input Voltage – All Other Inputs …….	-0.5V to VCC + 0.5V
DC Output Current – Outputs ……	24mA
DC Output Current – Low Impedance Bidirectionals ……...	24mA
Power Dissipation (VCC = 5.25V)…….	500mW

DC CHARACTERISITICS

(Ambient Temperature = -40°C to 85°C)

Operating Voltage and Current

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
Vcc1	VCC Operating Supply Voltage	3.3	-	5.25	V	
Vcc2	VIO Operating Supply Voltage	1.8	-	5.25	V	
Icc1	Operating Supply Current	-	15	-	mA	Normal Operation
Icc2	Operating Supply Current	50	70	100	uA	USB Suspend

FIFO Data / Control Bus I/O Pin Characteristics (VIO = 5V)

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
Voh	Output Voltage High	3.2	4.1	4.9	V	I source = 2 mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 2 mA
Vin	Input Switching Threshold	1.3	1.6	1.9	V	* Note 1
VHys	Input Switching Hysteresis	50	55	60	mV	* Note 1

* Note 1 – Inputs have an internal 200kΩ pull-up resistor to VIO

FIFO Data / Control Bus I/O Pin Characteristics (VIO = 3.3V)

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
Voh	Output Voltage High	2.2	2.7	3.2	V	I source = 1 mA
Vol	Output Voltage Low	0.3	0.4	0.5	V	I sink = 2 mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	* Note 1
VHys	Input Switching Hysteresis	20	25	30	mV	* Note 1

* Note 1 – Inputs have an internal 200kΩ pull-up resistor to VIO

FIFO Data / Control Bus I/O Pin Characteristics (VIO = 2.8V)

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
Voh	Output Voltage High	2.1	2.6	3.1	V	I source = 1 mA
Vol	Output Voltage Low	0.3	0.4	0.5	V	I sink = 2 mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	* Note 1
VHys	Input Switching Hysteresis	20	25	30	mV	* Note 1

- Note 1 – Inputs have an internal 200kΩ pull-up resistor to VIO

FIFO Data / Control Bus I/O Pin Characteristics (VIO = 5V, High Drive Level)

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
Voh	Output Voltage High	3.2	4.1	4.9	V	I source = 6 mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 6 mA
Vin	Input Switching Threshold	1.3	1.6	1.9	V	* Note 1
VHys	Input Switching Hysteresis	50	55	60	mV	* Note 1

* Note 1 – Inputs have an internal 200kΩ pull-up resistor to VIO

FIFO Data / Control Bus I/O Pin Characteristics (VIO = 3.3V, High Drive Level)

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
Voh	Output Voltage High	2.2	2.7	3.2	V	I source = 3 mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 8 mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	* Note 1
VHys	Input Switching Hysteresis	20	25	30	mV	* Note 1

* Note 1 – Inputs have an internal 200kΩ pull-up resistor to VIO

FIFO Data / Control Bus I/O Pin Characteristics (VIO = 2.8V, High Drive Level)

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
Voh	Output Voltage High	2.1	2.6	3.1	V	I source = 3 mA
Vol	Output Voltage Low	0.3	0.4	0.5	V	I sink = 8 mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	* Note 1
VHys	Input Switching Hysteresis	20	25	30	mV	* Note 1

* Note 1 – Inputs have an internal 200kΩ pull-up resistor to VIO

RSTI Pin Characteristics

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
Vin	Input Switching Threshold	1.1	1.5	1.8	V	
VHys	Input Switching Hysteresis		200		mV	

EEPROM RELIABILITY CHARACTERISITICS

Internal 1024 Bit EEPROM Characteristics

Parameter Description	*Value*	*Units*
Data Retention	15	Years
Read / Write Cycles	100,000	Cycles

INTERNAL CLOCK CHARACTERISITICS

Internal Clock Characteristics

Parameter	*Value*			
	Min	*Typ*	*Max*	*Units*
Frequency of Operation	11.98	12.00	12.02	MHz
Clock Period	83.19	83.33	83.47	ns
Duty Cycle	45	50	55	%

TECHNICAL SUPPORT AND FURTHER INFORMATION

For any questions relating to the USBMOD245R please contact us by Email, Fax or Phone.

Email: support@elexol.com

Ph: +61 755 031202
Fax: +61 755 031206

Elexol Pty Ltd
Unit 1
8 Pirelli Street, Southport
Queensland 4215
Australia

Elexol Pty Ltd
PO Box 2742
Southport Business Centre
Queensland 4215
Australia

PRODUCT USE LIMITATIONS, WARRANTY & QUALITY STATEMENT

The USBMOD245R should not be used in any situation where it's failure or failure of the PC or software controlling it could cause human injury or severe damage to equipment. This device is not designed for or intended to be used in any life critical application.

The USBMOD245R is warranted to be free from manufacture defects for a period of 12 months from the date purchase.
Subjecting the device to conditions beyond the Absolute Maximum Ratings listed above will invalidate this warranty.
The USBMOD245R is a static sensitive device, anti static procedures should be used in the handling of this device.

All USBMOD245R units are extensively tested at time of manufacture to be free of defects.

Elexol is committed to providing products of the highest quality. Should you experience any product quality issues with this product please contact our quality assurance manager at the above address.

DISCLAIMER

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